EXHIBIT A

UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

LIGHT SPEED MICROELECTRONICS, LLC, Plaintiff, v. NXP USA, INC. Defendant.	CIVIL ACTION FILE NO. 6:21-cv-00066-ADA **JURY TRIAL DEMANDED**

THIRD AMENDED COMPLAINT FOR PATENT INFRINGEMENT

1. This is an action for direct patent infringement under 35 U.S.C. § 271(a), by Light Speed Microelectronics, LLC ("LSM") against NXP USA, Inc. ("NXP"). This action is for infringement of at least Claim 23 of U.S. Patent No. 7,870,161 (the "161 Patent" **Exhibit A**), Claims 1-14 of U.S. Patent No. 10,860,832 (the "832 Patent" **Exhibit B**), and Claims 1-30 of U.S. Patent No. 10,949,641 (the "641 Patent" **Exhibit C**), both literally and under the doctrine of equivalents.

2. NXP's infringement is direct, resulting from use of the methods outlined and claimed in the 161 Patent, 832 Patent and 641 Patent (collectively, the "Asserted Patents"), as set forth in the claim charts attached as **Exhibits D-F**.

3. Linux board support packages (BSPs) for NXP's QorIQ processors featuring the Pattern Matching Engine 2.x ("PME") as part of the Data Path Acceleration Architecture (including at least the NXP P2040, P2041, P3041, P4040, P4080, P5010, P5020, T1020, T1022, T1040, T1042, T2080, T2081, T4080, T4160, T4240, LS2040A, LS2045A, LS2048, LS2080A, LS2085 and LS2088, and the reference boards for each of these processors (collectively, the "Accused

Instrumentalities")) are tested and certified by NXP, ensuring fully operational toolchain, kernel and board specific modules that are ready to use together within a fixed configuration for specific hardware reference platforms employing the Pattern Matching Engine 2.x to infringe the method claimed in the Asserted Patents.

4. For example, the method is specifically used by NXP in the manufacture, use and sale of reference boards for each of the referenced QorIQ processors within the Accused Instrumentalities, said reference boards being pre-loaded with the Embedded Linux® Essentials for QorIQ processors with data path acceleration software development kit.

5. Furthermore, Defendant's infringement is indirect by inducing infringement by, with knowledge of the Asserted Patents and infringement thereof, encouraging, aiding and abetting on an ongoing basis, including throughout this litigation, as further detailed herein.

THE PARTIES

6. LSM is a limited liability company formed under the laws of Texas with its registered office address located in Waco, Texas. LSM is the owner by assignment of all rights, title and interest in the Asserted Patents, including but not limited to seeking past, present and future damages, injunctive relief and all other relief sought herein.

7. NXP is a Delaware Corporation. It is registered to do business in Texas including in the name NXP Semiconductors USA, Inc.; operates at least in two Austin, Texas locations; and may be served through its registered agent at Corporate Service Company DBA CSC - Lawyers Inco. located at 211 E. 7th Street, Suite 620, Austin, Texas 78701.

8. NXP and its parent company together comprise one of the world's largest manufacturers of integrated circuits.

PERSONAL JURISDICTION AND VENUE

9. This is an action for infringement of a United States patent arising under 35 U.S.C. §§ 271, 281, and 284, among others. This Court has subject matter jurisdiction of the action under 28 U.S.C. §§ 1331 and 1338(a).

10. NXP has availed itself of the privilege of doing business in Texas, including in this judicial district. Upon information and belief, NXP has regular and established places of business in Texas, including within this judicial district.

11. Upon information and belief, NXP has hired employees who work in this judicial district who advance the manufacture and sale of the Accused Instrumentalities.

12. This Court has personal jurisdiction over NXP pursuant to due process and/or the Texas Long Arm Statute because, *inter alia*, (i) NXP has done and continues to do business in Texas; (ii) NXP has committed and continues to commit acts of patent infringement in the State of Texas, including making, using, offering to sell, and/or selling Accused Instrumentalities in Texas, and/or importing Accused Instrumentalities into Texas, including by Internet sales and sales via retail and wholesale stores, inducing others to commit acts of patent infringement in Texas, and/or committing a least a portion of any other infringements alleged herein; and (iii) NXP is registered to do business in Texas.

13. Venue is proper in this district as to NXP pursuant to 28 U.S.C. § 1400(b). Venue is further proper because NXP has committed and continues to commit acts of patent infringement in this district, including making products which perform in accordance with specific method claims of the Asserted Patents, using specific method claims of the Asserted Patents, offering to sell, and/or selling the Accused Instrumentalities in this district, and/or importing Accused Instrumentalities into this district, including by Internet sales and sales via retail and wholesale

stores, inducing others to commit acts of patent infringement in this district, and/or committing at least a portion of any other infringements alleged herein in this district. NXP also has a regular and established place of business in this district, including at least at 6501 W William Cannon Drive, Austin, TX 78735 and at 3501 Ed Bluestein Blvd., Austin, TX 78721, as stated on NXP's website:

https://www.nxp.com/company/our-company/about-nxp/worldwide-locations/nxp-in-the-united-states:USA

COUNT I

(Direct Infringement of and Inducement to Infringe the 161 Patent)

14. LSM incorporates herein by reference the contents of the preceding paragraphs 1-13 as if restated fully herein.

15. Public NXP technical documents establish that the making, offer to sell and sale of the Accused Instrumentalities infringe one or more claims of the 161 Patent, including at least claim 23, literally and/or under the Doctrine of Equivalents. This direct infringement is based on NXP's use of specific method claims of the 161 Patent, including in the making, use (including testing), sale of and offer to sell the Accused Instrumentalities in the United States.

Background

16. By way of background to the invention of the 161 Patent, data networks and the data that passes through them are important business assets. To help safeguard these assets and to process the data (strings of characters) passing through them properly, both the incoming and the outgoing data must be scanned at ever-increasing speeds to filter out unwanted content, flag important messages, and prevent unauthorized access. The scanning usually involves scanning the incoming data for patterns that may denote, for example, a virus or other unauthorized intrusion.

17. The above-referenced data patterns are also referred to as data signatures. Signature detection is the underlying technology behind Intrusion Detection, Intrusion Prevention (IDS/IPS), and Application Recognition systems. Signatures are patterns (e.g., data patterns), which when matched, indicate the system should apply designated security or Quality of Service ("QoS") policies.

18. The data signatures are reducible to binary strings which can be located by scanning the data, either in software or with specialized hardware accelerators. One major complexity in detecting binary strings is dealing with strings that are deliberately spread over multiple network datagrams, contain multiple character options (capitalization), or otherwise include wildcards. The language for defining data signatures is known as "Regular Expressions" and accelerators that scan data for signatures based on regular expression rules are often referred to as "RegEx Engines."

19. A workable scanning solution should be able to scan the data stream for multiple target patterns. Ideally, a single scan of a specified data set should be able to scan for such multiple target patterns. Performing multiple scans or passes through the data set would seriously degrade the performance of such a solution, where performance is a key concern.

20. Conventional software scanners, unfortunately, are known to be insufficient when it comes to scanning speed for high performance and/or high capacity applications. Furthermore, they require a large expenditure in terms of both hardware, software, and power. A hardware solution is faster and more efficient than a software solution.

NXP Data Path Acceleration Architecture with Pattern Matching Engines ("PME")

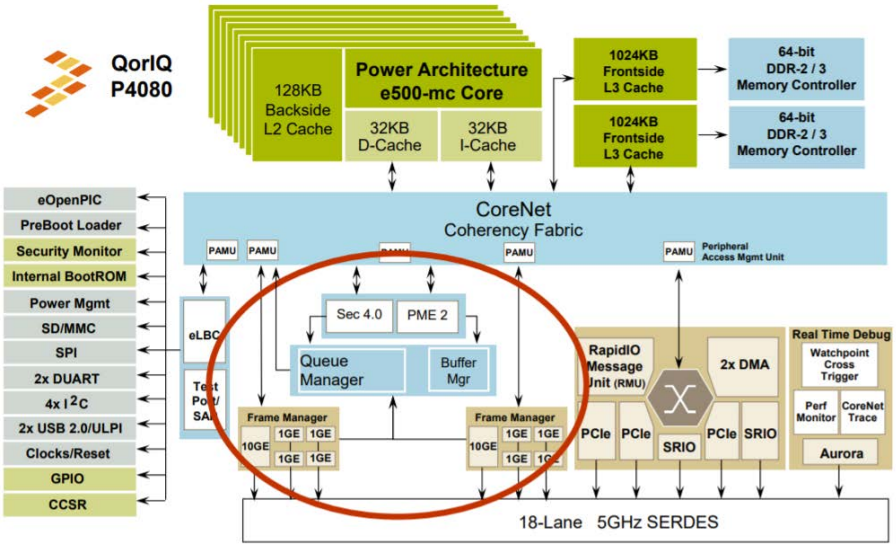
21. For certain processors (*e.g.*, QorIQ processors and related reference boards), NXP has designed a Data Path Acceleration Architecture (DPAA). The QorIQ DPAA is a comprehensive

architecture which integrates all aspects of packet processing in the SoC (system on chip), addressing issues and requirements resulting from the nature of the QorIQ multicore SoCs. The DPAA includes: cores; network and packet I/O; hardware offload accelerators; and the infrastructure required to facilitate the flow of packets between the above.

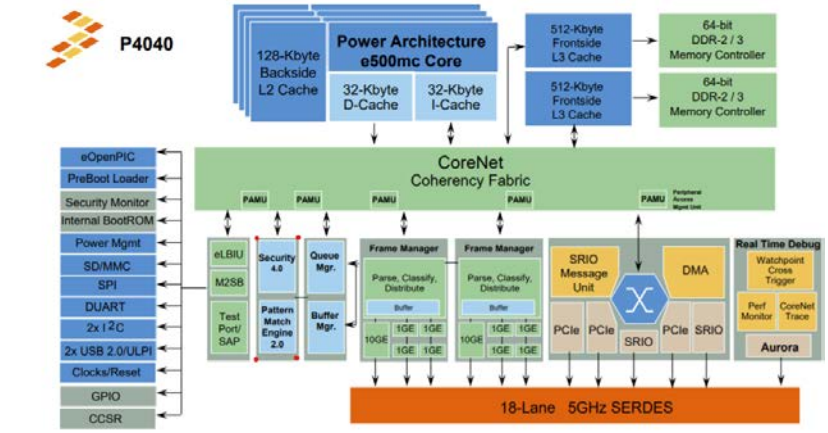
22. Within NXP's DPAA, there are two hardware accelerators: (1) SEC – cryptographic accelerator; and (2) PME – pattern matching engine. Cryptographic and pattern matching accelerators are examples of specific hardware offload engines that more effectively perform the kind of intensive, repetitive algorithms to be performed on large portions of incoming data stream(s) at high speeds in modern network applications. These hardware accelerators act as standalone hardware elements that are fed blocks or streams of data, perform the required processing, and then provide the output in a separate stream or data block within the system. The performance boost is significant for tasks that can be done by these hardware accelerators as compared to a software implementation.

23. The hardware accelerators are illustrated in the following diagrams of the DPAA components for various QorIQ systems-on-chip (SOCs):

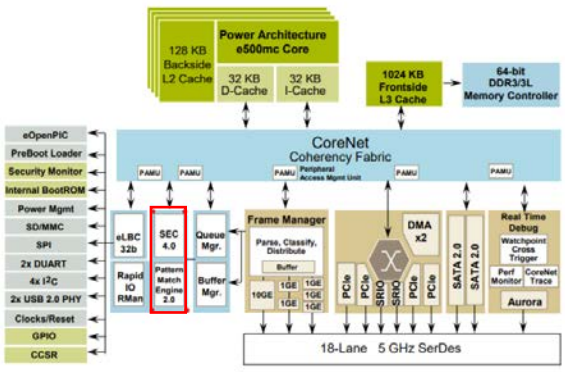
QorIQ P4080 DPAA Components



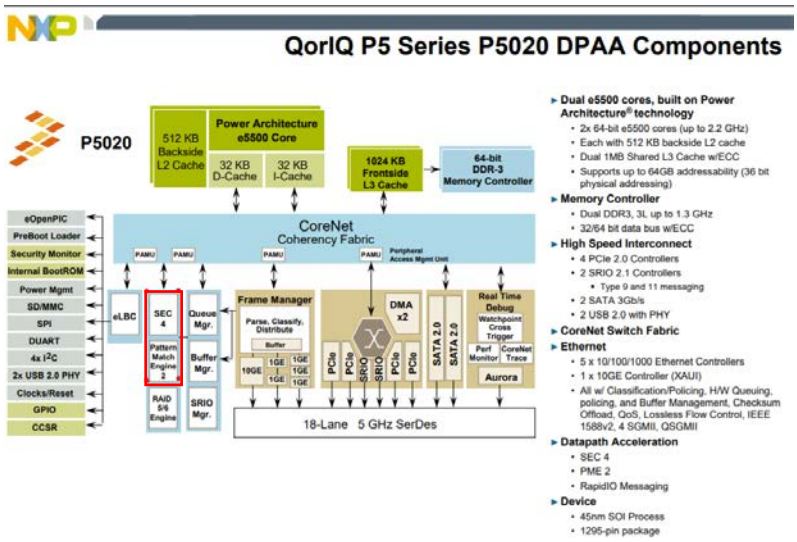
P4040 Block Diagram



QorIQ P3 Series P3041 Block Diagram

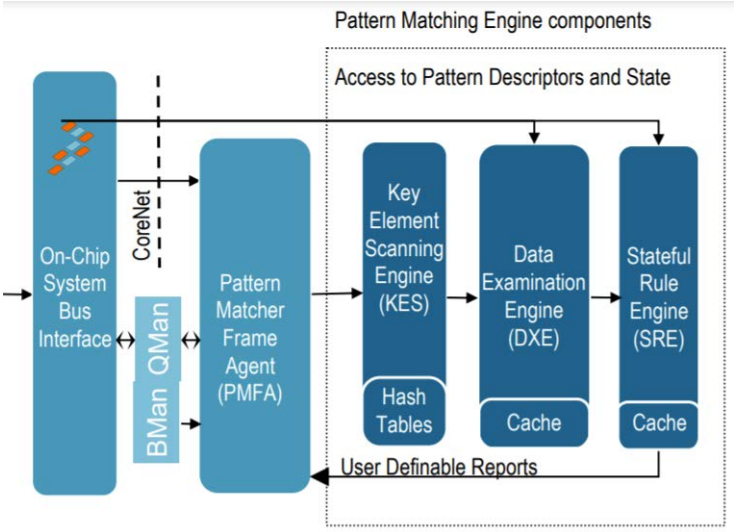


- **Quad e500mc cores, built on Power Architecture® technology**
  - 4 cores (up to 1.5 GHz)
  - Each with 128KB backside L2 cache
  - 1MB Shared L3 Cache w/ECC
- **Memory Controller**
  - DDR3/3L SDRAM up to 1.3 GHz
  - 32/64 bit data bus w/ECC
- **High Speed Interconnect**
  - 4 PCIe 2.0 Controllers
  - 2 SRIO 2.1 Controllers
    - Type 9 and 11 messaging
  - 2 SATA 2.0
- **CoreNet Switch Fabric**
- **Ethernet**
  - 5 x 10/100/1000 Ethernet Controllers
    - Or 4x 2.5Gb/s SGMII
  - 1 x 10GE Controllers
  - All w/ Classification, H/W Queueing, policing, and Buffer Management, Checksum Offload, QoS, Lossless Flow Control, IEEE 1588
  - Up to 1 XAUI, 4 SGMII or 2.5Gb/s SGMII, 2 RGMII
- **Device**
  - 45nm SOI Process
  - 1295-pin package, pin compat with P4040
    - 37.5x37.5mm



24. The Accused Instrumentalities are NXP processors and related reference boards employing the PME, which provides for a method for string signature scanning for one or more fully specified signatures. The advantages of the NXP PME include: (a) the use of a fast pre-scan to determine which incoming strings require greater scrutiny; and (b) the inclusion of on-chip hash tables for low system memory utilization in the fast pre-scan process, removing the need for more costly low-latency memory technologies.

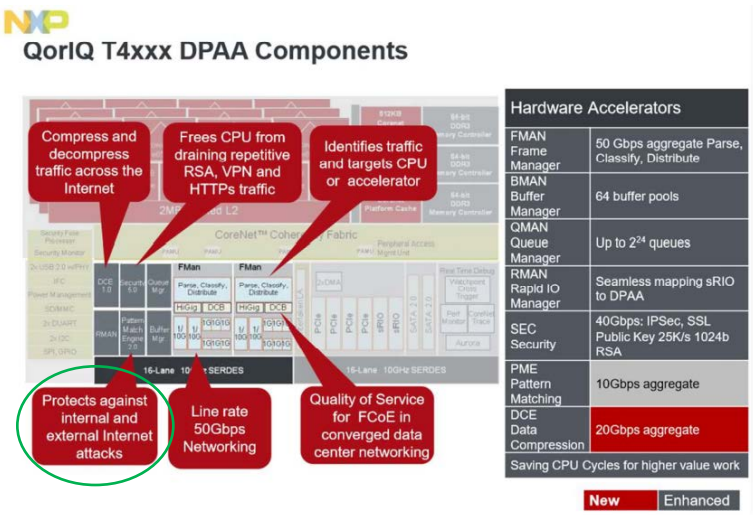
25. The PME utilizes a pipeline of processing blocks to provide a complete pattern matching solution, illustrated as follows:



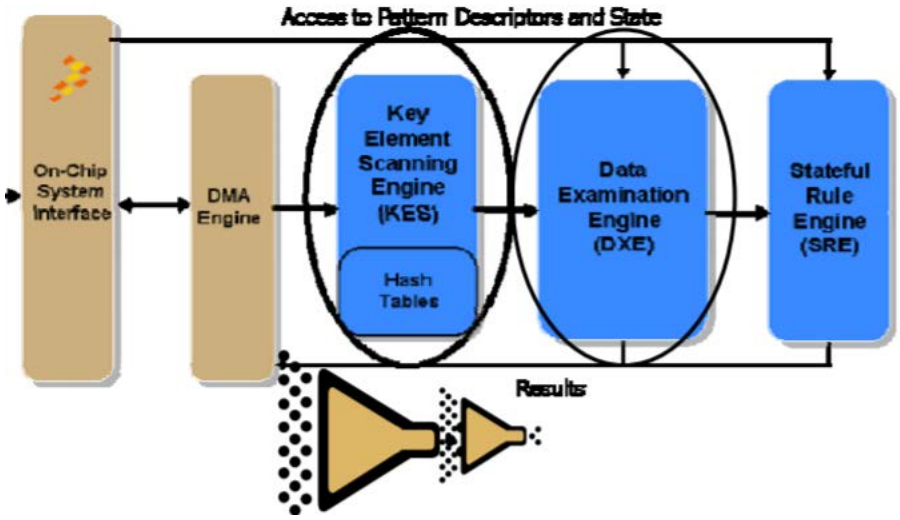
26. The PME is a hardware accelerator used to conduct a fast scan of incoming data strings to identify any strings bearing target signatures. PME provides for the processing of one or more signatures into one or more formats including selecting a fingerprint for each signature. For example, each pattern (*i.e.* the "signature" recited in the claim) is processed into multiple formats, including: "Key Element," "fingerprint," "fingerprint hash," a "pre-computed hash value of the Key Element," and at least one of "Original Byte," "Equivalent Byte," "Pre-Defined Group," and "User-Defined Group," as used in the Data Examination Engine ("DXE").

27. PME offers what is called "Regex support" (meaning that it supports signature matching based on regular expression or "Regex" signature patterns), with these extensions: (1) patterns can be split into 256 sets each of which can contain 16 subsets; (2) 32K patterns of up to 128B length are supported; and (3) it offers 9.6 Gbps raw performance. PME utilizes a pipeline of processing blocks to provide these capabilities and a complete pattern matching solution.

28. PME combines hash and Non-deterministic Finite Automaton ("NFA") technology, with no "explosion" in the number of patterns due to wildcards, low system memory utilization, and incorporation of a fast pattern database that allows compiling and incrementally updating target signatures against which incoming character strings are scanned. The PME is used to identify malicious character strings, and to protect against internal and external Internet attacks. The following NXP diagram shows this point:



29. The PME processes one or more signatures into one or more formats including constructing one or more search data structures for the one or more fingerprints associated with the one or more signatures including hashing the fingerprints using one or more hash functions including forming one or more hash tables (shown in the diagram below), including a Variable Length Trigger (VLT) hash table from an uncompressed VLT table comprising bits used to indicate whether a pattern exists for a given hash values. The PME does this by employing a Key Element Scanning Engine ("KES"), which scans data, including the string under inspection ("SUI"), against at least one hash table looking for potential pattern matches. KES filters the work to be performed by the DXE by sending the strings under inspection containing potential pattern matches (as opposed to all strings under inspection), illustrated as follows:



30. In the PME, every pattern has an associated fingerprint. A fingerprint for a pattern is a set of contiguous symbols of type "Equivalent Byte" of length 1, 2, or K (from 2 to 16). The PME starts pattern searches in the input data relative to the position of the pattern fingerprints in the input data. KES computes a hash for different fingerprint lengths and looks up on-chip hash tables. A "hit" on one of these hashes results in a second level filter (called a "confidence" hash) being performed.

31. The PME provides for the processing of one or more signatures into one or more formats including constructing one or more follow-on search data structures, including the use of "Compare Types" in the DXE, consisting of "Original Byte," "Equivalent Byte," "Pre-Defined Group," and "User-Defined Group." The DXE performs complete match for each "possible" match found by KES. From the perspective of the DXE, each pattern is an independent description (set of specialized instructions) of related symbol comparisons that are applied relative to a specific anchor position of a given SUI. The symbol comparisons are evaluated (using NFA) as defined by the description and this evaluation results in either a match or a non-match indication.

32. In the PME, as discussed above, a fingerprint for a pattern may include contiguous symbols comprising at least a portion of a Key Element, such that each fingerprint includes a fragment of a particular Regex signature. Table 10-121 below shows for each Regex an exemplary Key Element. The PME does not limit the position of the Key Element, and therefore, the symbols of the Key Element can be anywhere within a given Regex signature pattern.

Table 10-121. Key Element Regex Syntax Examples

Regex Syntax	Key Element
ABCDXYZ	ABCDXYZ
ABC[0-9]XYZ	ABC_XYZ
ABC(EFG|JKL)XYZ	ABC_XYZ
ABC(EFG|JKLM)XYZ	ABC or XYZ
ABC(XYZ|JKL)	ABC
ABCD{2,5}XYZ	Either ABCDD or DDXYZ
(ABC|DEF)(QRS|XYZ)	Regular expression split required: ABC(QRS|XYZ) with a Key Element of ABC DEF(QRS|XYZ) with a Key Element of DEF
ABC(QRS|XYZ)	ABC
DEF(QRS|XYZ)	DEF
[Aa][Bb][Cc]	[Aa][Bb][Cc]
[Aa]bc	[Aa]bc

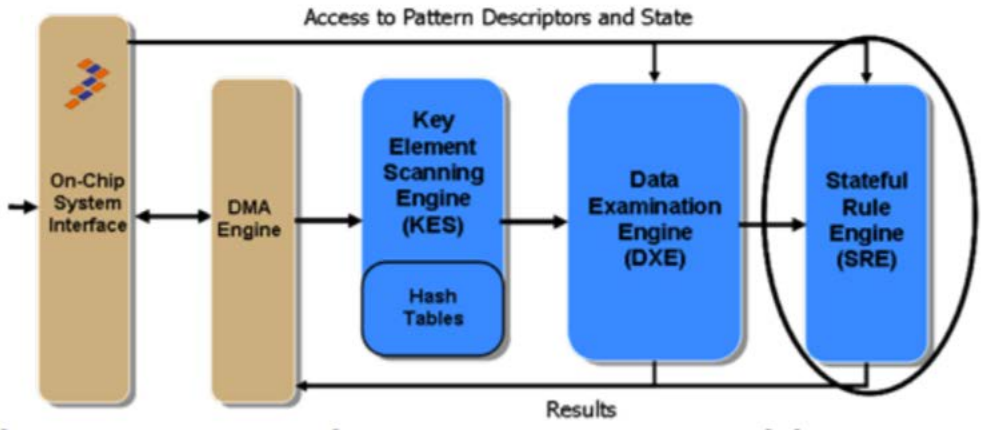
33. The PME receives a particular string field comprising a string of data values. For instance, the purpose of the KES is to pre-scan the SUI data using internal hash tables and to identify, at each alignment within the SUI, the patterns that could possibly produce a positive match using the DXE. The SUI is an example of a particular string field comprising a string of data values.

34. The PME identifies any signatures included in the particular string field including scanning the particular string field for the one or more fingerprints associated with the one or

more signatures at each. This also includes the hashing of one or more data samples of the particular string field of one or more sizes of the one or more fingerprints using the one or more hash functions to generate one or more hash values and querying the one or more search data structures for the one or more fingerprints using the one or more hash values. The KES of the PME performs these functions. In KES, for example, the KES Trigger stage detects the possibility of a pattern match by detecting the possibility of a fingerprint of a pattern or a position at which a pattern may be anchored. It performs this function by hashing of one or more data samples of the particular string field of one or more sizes of the one or more fingerprints using the one or more hash functions to generate one or more hash values and querying the one or more search data structures for the one or more fingerprints using the one or more hash values, executing multiple look-up methods (*e.g.*, 1-Byte Trigger, 2-Byte Trigger, Variable Length Trigger look ups) in parallel for each SUI alignment.

35. The PME searches the particular string field for the one or more signatures associated with one or more identified fingerprints using the one or more follow-on search data structures at the locations where the one or more identified fingerprints are found including identifying any potential signatures included in the particular string field for the one or more signatures associated with the one or more identified fingerprints and comparing one or more identified potential signatures with the particular string field at the locations where the one or more identified potential signatures are found. The DXE of the PME performs these functions.

36. The PME includes the outputting of any identified signatures in the particular string field. This output includes the pattern matches identified by the DXE and outputted to the Stateful Rules Engine (SRE) to further qualify pattern matches, illustrated as follows:



37. The claim chart attached as Exhibit D hereto illustrates further that, based on the foregoing, all elements of at least one claim of the 161 Patent are present in each of the Accused Instrumentalities. Because all elements of at least one claim of the 161 Patent are present in each of the Accused Instrumentalities, either literally or, if not literally, at a minimum under the doctrine of equivalents, NXP's manufacture, use (including testing), past and present sales and offers for sale of the Accused Instrumentalities directly infringe at least one claim of the 161 Patent.

38. NXP was first placed on notice of a claim of infringement of the 161 Patent at least as early as January 29, 2021.

39. Since at least as early as January 29, 2021, NXP has also induced one or more third parties, including, upon information and belief, Cisco, Broadcom (formerly Brocade) and Juniper Networks, into infringement of the 161 Patent with knowledge of the 161 Patent, by encouraging, aiding and abetting said third parties to infringe on an ongoing basis, including throughout this litigation, by virtue of, *inter alia*, aiding and abetting consumers to buy and use the aforementioned QorIQ processors featuring the PME in the United States in accordance with the methods of the Asserted Claims. This inducement by NXP includes, but is not limited to:

(1) the utilization of customer support for use of the PME on the aforementioned QorIQ processors, including providing customers with access to a Linux software development kit (SDK) for the aforementioned QorIQ processors, including a Linux kernel driver and a Pattern Matching Engine (PME) driver library for US Data Path Acceleration Architecture (USDPAA), to better enable them to practice the 161 Patent, as well as written materials instructing and advising customers of the use of the PME;

(2) contributing to customers' and potential customers' enablement software drivers for the platforms of the QorIQ customers, including drivers enabling PME, into publicly available communities like kernel.org, and uboot, among others, whereupon customers of the aforementioned QorIQ processors can access and utilize them freely to practice the 161 Patent;

(3) contributing to customers' and potential customers' enablement software for the PME with the foregoing QorIQ processors, including but not limited to drivers such as a pattern matching (PM) driver, a PM Control Interface, a Regex compiler and a Stateful-Rule compiler, a Linker Loader and a Pattern Matcher (PM) Manager application, whereupon customers of the aforementioned QorIQ processors can access and utilize them freely to practice the methods of the Asserted Claims;

(4) publishing and maintaining content, including diagrams, release notes and other documentation on the web site NXP.com and docs.nxp.com used to educate and encourage customers regarding use of the PME within the framework of the QorIQ processor's DPAA to perform the methods of the Asserted Claims. This includes, for example, the maintenance of a user's guide written for programmers developing software for a QorIQ processor equipped with the PME hardware, said user guide describing the supplied pattern matcher software components, how to use the various application programming interfaces of the PME, and how to

integrate the resulting customized software. For example, sample Pattern Matcher applications are described in this document, whereupon customers of the aforementioned QorIQ processors and reference boards can access and utilize them freely to practice the 161 Patent;

(5) making available to customers and potential customers a SNORT PM plugin and other executables that enable the functionality of the PME without the need for the full Linux SDK, whereupon customers of the aforementioned QorIQ processors can access and utilize them freely to practice the 161 Patent;

(6) selling, offering to sell, marketing and supporting reference boards for each of the aforementioned QorIQ processors, pre-loaded with the DPAA software development kit, including the SDK enabling PME, which are sold and otherwise distributed to promote the sale and usage of the QorIQ processors, whereupon customers of the aforementioned reference boards can access and utilize them freely to practice the 161 Patent.

40. As a result of the infringement of the 161 Patent, LSM has been damaged and is entitled to recovery damages in an amount not less than a reasonable royalty.

COUNT II
(Direct Infringement of and Inducement to Infringe the 832 Patent)

41. LSM incorporates herein by reference the contents of the preceding paragraphs 1-40 as if restated fully herein.

42. Public NXP technical documents establish that the making, offer to sell and sale of the Accused Instrumentalities infringe one or more claims of the 832 Patent, including at least claims 1-14, literally and/or under the Doctrine of Equivalents. This direct infringement is based on NXP's use of specific method claims of the 832 Patent, including in the making, use (including testing), sale of and offer to sell the Accused Instrumentalities in the United States.

43. The claim chart attached as Exhibit E hereto illustrates further that, based on the foregoing, all elements of at least one claim of the 832 Patent are present in each of the Accused Instrumentalities as made, used, sold and/or offered for sale. Because all elements of at least one claim of the 832 Patent are present in each of the Accused Instrumentalities, either literally or, if not literally, at a minimum under the doctrine of equivalents, NXP's manufacture, use (including testing), past and present sales and offers for sale of the Accused Instrumentalities directly infringe at least one claim of the 832 Patent.

44. NXP was first placed on notice of a claim of infringement of the 832 Patent at least as early as January 29, 2021.

45. Since at least as early as January 29, 2021, NXP has also induced one or more third parties, including, upon information and belief, Cisco, Broadcom (formerly Brocade) and Juniper Networks, into infringement of the 832 Patent with knowledge of the 832 Patent, by encouraging, aiding and abetting said third parties to infringe on an ongoing basis, including throughout this litigation, by virtue of, *inter alia*, aiding and abetting consumers to buy and use the aforementioned QorIQ processors featuring the PME in the United States in accordance with the methods of the Asserted Claims. This inducement by NXP includes, but is not limited to:

(1) the utilization of customer support for use of the PME on the aforementioned QorIQ processors, including providing customers with access to a Linux software development kit (SDK) for the aforementioned QorIQ processors, including a Linux kernel driver and a Pattern Matching Engine (PME) driver library for US Data Path Acceleration Architecture (USDPAA), to better enable them to practice the 832 Patent, as well as written materials instructing and advising customers of the use of the PME;

(2) contributing to customers' and potential customers' enablement software drivers for the platforms of the QorIQ customers, including drivers enabling PME, into publicly available communities like kernel.org, and uboot, among others, whereupon customers of the aforementioned QorIQ processors can access and utilize them freely to practice the 832 Patent;

(3) contributing to customers' and potential customers' enablement software for the PME with the foregoing QorIQ processors, including but not limited to drivers such as a pattern matching (PM) driver, a PM Control Interface, a Regex compiler and a Stateful-Rule compiler, a Linker Loader and a Pattern Matcher (PM) Manager application, whereupon customers of the aforementioned QorIQ processors can access and utilize them freely to practice the claims of the 832 Patent;

(4) publishing and maintaining content, including diagrams, release notes and other documentation on the web site NXP.com and docs.nxp.com used to educate and encourage customers regarding use of the PME within the framework of the QorIQ processor's DPAA to perform the methods of the Asserted Claims. This includes, for example, the maintenance of a user's guide written for programmers developing software for a QorIQ processor equipped with the PME hardware, said user guide describing the supplied pattern matcher software components, how to use the various application programming interfaces of the PME, and how to integrate the resulting customized software. For example, sample Pattern Matcher applications are described in this document, whereupon customers of the aforementioned QorIQ processors and reference boards can access and utilize them freely to practice the claims of the 832 Patent;

(5) making available to customers and potential customers a SNORT PM plugin and other executables that enable the functionality of the PME without the need for the full Linux

SDK, whereupon customers of the aforementioned QorIQ processors can access and utilize them freely to practice the claims of the 832 Patent;

(6) selling, offering to sell, marketing and supporting reference boards for each of the aforementioned QorIQ processors, pre-loaded with the DPAA software development kit, including the SDK enabling PME, which are sold and otherwise distributed to promote the sale and usage of the QorIQ processors, whereupon customers of the aforementioned reference boards can access and utilize them freely to practice the claims of the 832 Patent.

46. As a result of the infringement of the 832 Patent, LSM has been damaged and is entitled to recovery damages in an amount not less than a reasonable royalty.

COUNT III
(Direct Infringement of and Inducement to Infringe the 641 Patent)

47. LSM incorporates herein by reference the contents of the preceding paragraphs 1-46 as if restated fully herein.

48. Public NXP technical documents establish that the making, offer to sell and sale of the Accused Instrumentalities infringe one or more claims of the 641 Patent, including at least claims 1-30, literally and/or under the Doctrine of Equivalents. This direct infringement is based on NXP's use of specific method claims of the 641 Patent, including in the making, use (including testing), sale of and offer to sell the Accused Instrumentalities in the United States.

49. The claim chart attached as Exhibit F hereto illustrates further that, based on the foregoing, all elements of at least one claim of the 641 Patent are present in each of the Accused Instrumentalities as made, used, sold and/or offered for sale. Because all elements of at least one claim of the 641 Patent are present in each of the Accused Instrumentalities, either literally or, if not literally, at a minimum under the doctrine of equivalents, NXP's manufacture, use (including

testing), past and present sales and offers for sale of the Accused Instrumentalities directly infringe at least one claim of the 641 Patent.

50. NXP was first placed on notice of claims 1-30 of infringement of the 641 Patent at least as early as July 26, 2021.

51. Since at least as early as January 29, 2021, NXP has also induced one or more third parties, including, upon information and belief, Cisco, Broadcom (formerly Brocade) and Juniper Networks, into infringement of the 641 Patent with knowledge of the 641 Patent, by encouraging, aiding and abetting said third parties to infringe on an ongoing basis, including throughout this litigation, by virtue of, *inter alia*, aiding and abetting consumers to buy and use the aforementioned QorIQ processors featuring the PME in the United States in accordance with the methods of the Asserted Claims. This inducement by NXP includes, but is not limited to:

(1) the utilization of customer support for use of the PME on the aforementioned QorIQ processors, including providing customers with access to a Linux software development kit (SDK) for the aforementioned QorIQ processors, including a Linux kernel driver and a Pattern Matching Engine (PME) driver library for US Data Path Acceleration Architecture (USDPAA), to better enable them to practice the 641 Patent, as well as written materials instructing and advising customers of the use of the PME;

(2) contributing to customers' and potential customers' enablement software drivers for the platforms of the QorIQ customers, including drivers enabling PME, into publicly available communities like kernel.org, and uboot, among others, whereupon customers of the aforementioned QorIQ processors can access and utilize them freely to practice the 641 Patent;

(3) contributing to customers' and potential customers' enablement software for the PME

with the foregoing QorIQ processors, including but not limited to drivers such as a pattern matching (PM) driver, a PM Control Interface, a Regex compiler and a Stateful-Rule compiler, a Linker Loader and a Pattern Matcher (PM) Manager application, whereupon customers of the aforementioned QorIQ processors can access and utilize them freely to practice the claims of the 641 Patent;

(4) publishing and maintaining content, including diagrams, release notes and other documentation on the web site NXP.com and docs.nxp.com used to educate and encourage customers regarding use of the PME within the framework of the QorIQ processor's DPAA to perform the methods of the Asserted Claims. This includes, for example, the maintenance of a user's guide written for programmers developing software for a QorIQ processor equipped with the PME hardware, said user guide describing the supplied pattern matcher software components, how to use the various application programming interfaces of the PME, and how to integrate the resulting customized software. For example, sample Pattern Matcher applications are described in this document, whereupon customers of the aforementioned QorIQ processors and reference boards can access and utilize them freely to practice the claims of the 641 Patent;

(5) making available to customers and potential customers a SNORT PM plugin and other executables that enable the functionality of the PME without the need for the full Linux SDK, whereupon customers of the aforementioned QorIQ processors can access and utilize them freely to practice the claims of the 641 Patent;

(6) selling, offering to sell, marketing and supporting reference boards for each of the aforementioned QorIQ processors, pre-loaded with the DPAA software development kit, including the SDK enabling PME, which are sold and otherwise distributed to promote the sale

and usage of the QorIQ processors, whereupon customers of the aforementioned reference boards can access and utilize them freely to practice the claims of the 641 Patent.

52. As a result of the infringement of the 641 Patent, LSM has been damaged and is entitled to recovery damages in an amount not less than a reasonable royalty.

PRAYER FOR RELIEF

WHEREFORE, LSM respectfully requests the Court to enter judgment as follows:

A. That NXP has directly infringed the Asserted Patents;

B. That NXP be ordered to pay damages adequate to compensate LSM for its infringement of the Asserted Patents, but in no event less than a reasonable royalty, together with prejudgment and post-judgment interest thereon;

C. That NXP be ordered to account for any post-verdict infringement and pay no less than a reasonable royalty, together with interest, thereon; and

D. That LSM be granted such other and additional relief as the Court deems just and proper.

JURY DEMAND

LSM hereby demands a jury trial as to all issues so triable.

DATED this 9th day of August, 2021.

RESPECTFULLY SUBMITTED,

/s/ Steven G. Hill
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